





EH39 45

Series — RoHS Compliant (Pb-free) 1.8V 4 Pad 3.2mm x 5mm Ceramic SMD LVCMOS Oscillator

Frequency Tolerance/Stability ______ ±50ppm Maximum

Operating Temperature Range - 0°C to +70°C

TS -7.3728M

Nominal Frequency 7.3728MHz

Pin 1 Connection
Tri-State (High Impedance)

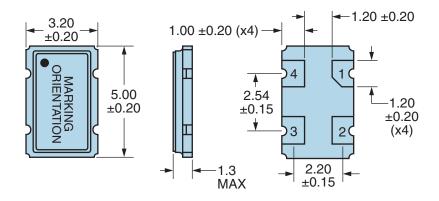
- Duty Cycle 50 ±10(%)

Operating 260°C R #5ppm/Y perating Temperature Range 0°C to + pply Voltage 1.8Vdc ± put Current 3.5mA M Itput Voltage Logic High (Voh) 90% of M Itput Voltage Logic Low (Vol) 10% of M Se/Fall Time 6nSec M Ity Cycle 50 ±10(9) ad Drive Capability 15pF Ma Itput Logic Type CMOS	Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the g Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°, eflow, Shock, and Vibration) Year Maximum 70°C
Operating 260°C R #5ppm/Y perating Temperature Range O°C to +1 pply Voltage Out Current Atput Voltage Logic High (Voh) ### 10% of Voltage Logic Low (Vol) #### 6nSec M ###################################	g Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°, eflow, Shock, and Vibration) 'ear Maximum 70°C -5% laximum (No Load) 'dd Minimum (IOH = -8mA)
perating Temperature Range 0°C to + pply Voltage 1.8Vdc ± 3.5mA M ptput Voltage Logic High (Voh) 10% of M ptput Voltage Logic Low (Vol) 10% of M ptput Voltage Logic Low (Vol) 10% of M ptput Voltage Logic Low (Vol) 15pF Ma ptput Logic Type 0°C to + 10% of M ptput Voltage Logic High (Voh) ptput Voltage Logic Low (Vol) 15pF Ma ptput Logic Type 0°C to + 10% of M ptput Voltage Logic High (Voh) ptput Voltage Logic Low (Vol) ptput Voltage Logic Low (70°C :5% aximum (No Load) /dd Minimum (IOH = -8mA)
pply Voltage 1.8Vdc ± out Current 3.5mA M stput Voltage Logic High (Voh) 10% of V se/Fall Time 6nSec M sty Cycle 50 ±10(9 ad Drive Capability 15pF Ma stput Logic Type 1.8Vdc ± 1.8	/dd Minimum (IOH = -8mA)
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ttput Voltage Logic High (Voh) 10% of Voltage Logic Low (Vol) 10% of Voltage Logic Low (Vol) 50 ±10(9 ad Drive Capability 15pF Ma 1tput Logic Type 150 ± 00(9)	/dd Minimum (IOH = -8mA)
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se/Fall Time 6nSec M ity Cycle 50 ±10(% ad Drive Capability 15pF Ma itput Logic Type CMOS	/dd Maximum (IOL = +8mA)
ty Cycle 50 ±10(9 ad Drive Capability 15pF Ma ttput Logic Type CMOS	
ad Drive Capability 15pF Ma httput Logic Type CMOS	aximum (Measured at 20% to 80% of waveform)
tput Logic Type CMOS	6) (Measured at 50% of waveform)
	ximum
n 1 Connection Tri-State	
	(High Impedance)
-State Input Voltage (Vih and Vil) 90% of \inpedan	dd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High ce)
andby Current 10µA Ma	ximum (Pin 1 = Ground)
solute Clock Jitter ±100pSe	ec Maximum
art Up Time 10mSec	Maximum
orage Temperature Range -55°C to	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS			
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V		
Fine Leak Test	MIL-STD-883, Method 1014, Condition A		
Flammability	UL94-V0		
Gross Leak Test	MIL-STD-883, Method 1014, Condition C		
Mechanical Shock	MIL-STD-883, Method 2002, Condition B		
Moisture Resistance	MIL-STD-883, Method 1004		
Moisture Sensitivity	J-STD-020, MSL 1		
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K		
Resistance to Solvents	MIL-STD-202, Method 215		
Solderability	MIL-STD-883, Method 2003		
Temperature Cycling	MIL-STD-883, Method 1010, Condition B		
Vibration	MIL-STD-883, Method 2007, Condition A		



MECHANICAL DIMENSIONS (all dimensions in millimeters)

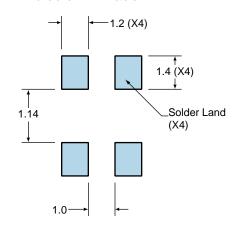


PIN	CONNECTION
1	Tri-State
2	Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	EPO
<u> </u>	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters



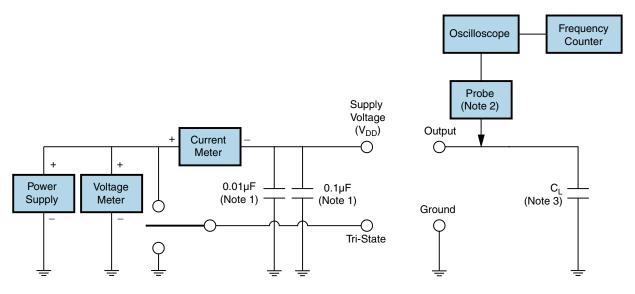
All Tolerances are ±0.1



OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for CMOS Output



- Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

 Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T _s MAX to T _∟ (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _S MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T _S MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	N/A
- Temperature Typical (T _S TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	240°C Maximum
Target Peak Temperature (T _P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.